REMARKS

In response to the Office Action mailed March 20, 2007, Applicant respectfully requests reconsideration. Claims 1-17 were previously pending in this application, with claims 1-6 and 12 having been withdrawn from consideration. Claims 7, 9 and 11 have been amended herein solely for the purpose of clarification. As a result, claims 7-11 and 13-17 are pending for examination with claims 7, 9, and 11 being independent. No new matter has been added by the amendments presented herein.

Status of Drawings

As a preliminary matter, Applicant notes that the Office Action Summary page indicates that the drawings filed on July 7, 2003 are objected to, yet no objection to the drawings is explained in the text of the Office Action. Applicant respectfully requests clarification.

Rejections Under 35 U.S.C. §112

The Office Action rejected claims 7-11 and 13-17 under 35 U.S.C. §112, first and second paragraphs. Applicant respectfully requests reconsideration.

1. Rejections under 35 U.S.C. §112, first paragraph

The Office Action alleges: "There is no support for a circuit comprising insulating portions covering the edges of the metal regions of determined pairs, wherein the edges of at least one pair of the metal regions not being covered by the insulating portions, as recite in claim 7 [sic], since the insulating portions covering all the edges of the metal regions of determined pairs, as depicted in figure 1D." (Page 2, third paragraph). Applicant respectfully disagrees. However, claim 7 has been amended herein for clarity. As amended, this portion of claim 7 now recites "insulating portions covering the facing edges of the metal regions of determined pairs according to the specific needs and not covering the facing edges of the metal regions of at least one pair other than the determined pairs." Support for the recitation of claim 7 is provided, without limitation, at FIG. 1D of the present application. FIG. 1D illustrates one embodiment of the invention in which an insulating portion 30 covers the facing edges of the metal regions 16C and 16D, but an insulating portion does not cover the facing edges of the metal regions 16A and 16B of at least one pair 16A and 16B other than the determined pairs (e.g., the pair of metal

regions 16C and 16D). Accordingly, Applicant respectfully requests that these rejections of claims 7 and 9 be withdrawn.

The Office Action further alleges: "There is no adequate description in the disclosure for the claimed limitations of 'at least one insulating portion covering the facing edges of at least one first pair of the pairs of metal regions so as to encode at least one first bit having a first polarity; and metal portions that cover the facing edges of at least one second pair of the pairs of metal regions so as to encode at least one second bit having a second polarity', as recited in claim 11." (Page 2, last paragraph). Applicant respectfully disagrees. However, claim 11 has been amended herein for clarity. Support for the recitation of claim 11 is provided, without limitation, at FIG. 1D of the present application. FIG. 1D illustrates one embodiment in which at least one insulating portion 30 covers the facing edges of at least one first pair 16C and 16D of the pairs of metal regions 16A-D, and a metal portion 20A that covers the facing edges of at least one second pair 16CA and 16B of the pairs of metal regions 16A-D. Furthermore, the specification of the present application clearly describes the encoding of data bits. For example, the specification includes the following paragraphs.

> Metal portion 28A performs an electric connection between metal regions 16A, 16B and thus closes the corresponding "anti-fuse". As an example, in the case where metal portion 16A is grounded and metal portion 16B is connected to a high voltage via a resistor, the coded information corresponds to a bit "0".
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> Similarly, metal regions 16C, 16D remain insulated from each other and thus form an open anti-fuse. In the case where one of the metal regions is grounded and the other one is connected to a high voltage, the coded information corresponds to a bit "1". (Page 5, line 28 to Page 6, line 2).

Therefore, the present application provides substantial written description to support the limitations of claim 11. Accordingly, Applicant respectfully requests that this rejection of claim 11 be withdrawn.

2. Rejections under 35 U.S.C. §112, second paragraph

With respect to claims 7 and 9, the Office Action states that it is unclear as to which element the second instance of the term "comprising" refers. In response, Applicant has amended claims 7 and 9 to clarify that the second instance of the term "comprising" refers to the integrated circuit.

Further with respect to claims 7 and 9, the Office Action states that it is unclear which element is the "associated covering metal portion," and how the phrase "at least one pair of metal regions" modifies the claimed structure. In response, Applicant has amended claims 7 and 9 for clarity. In particular, claim 7 has been amended to delete the term "associated covering metal portion," and to clarify that one of the metal portions is associated with a determined pair.

The Office Action further alleges that it is "unclear as to the exact location of the insulating portions associated with the determined pairs." Applicant respectfully disagrees. Claim 7 specifically recites the location of the insulating portion. Claim 7 as amended recites, *inter alia*, "each of the insulating portions being interposed between the facing edges of the metal regions of a determined pair and a covering one of the metal portions that is associated with the determined pair."

With respect to claim 11, the Office Action alleges that it is unclear as to what is meant by encoding bits of first and second polarities. Although Applicant respectfully disagrees, claim 11 has been amended to clarify that the first and second bits have opposite binary values (e.g., the binary values zero and one).

The Office Action further alleges that it is unclear how bits are encoded by the insulating and metal portions. As discussed above, the specification describes an embodiment in which bits are encoded in the following manner.

> Metal portion 28A performs an electric connection between metal regions 16A, 16B and thus closes the corresponding "anti-fuse". As an example, in the case where metal portion 16A is grounded and metal portion 16B is connected to a high voltage via a resistor, the coded information corresponds to a bit "0".
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> Similarly, metal regions 16C, 16D remain insulated from each other and thus form an open anti-fuse. In the case where one of the metal regions is grounded and the other one is connected to a high voltage, the coded information corresponds to a bit "1". (Page 5, line 28 to Page 6, line 2).

In this embodiment, the presence of an insulating portion 30 insulates the facing metal regions 16A and 16B from the metal portion 28B. As a result, metal regions 16A and 16B remain insulated from one another with a voltage difference between them, thus encoding a bit "1."

For facing metal regions 16A and 16B, the absence of an insulating portion (e.g., the absence of an insulating portion similar to region 30) allows a connection between metal regions

16A and 16B through metal portion 28A. The presence of an electrical connection through metal portion 28A keeps both 16A and 16B at the same voltage, thus encoding a "0." .

In view of the amendments to claims 7, 9 and 11 and the foregoing remarks, Applicant believes that the rejections under 35 U.S.C. §112 have been overcome. Accordingly, Applicant respectfully requests that the rejections of claims 7-11 and 13-17 under 35 U.S.C. §112 be withdrawn.

Rejections Under 35 U.S.C. §102

The Office Action rejected claims 7-10 under 35 U.S.C. §102(e) as being purportedly anticipated by Ishimaru (U.S. Patent No. 6,656,826). Applicants respectfully request reconsideration.

1. Discussion of Ishimaru

Ishimaru relates to a semiconductor device that has a fuse to be blown by an energy beam (Abstract). FIG. 1 illustrates a fuse area 12 that includes two copper regions 2 connected by a refractory metal film 8 and an aluminum film 9. The fuse is blown by directing a laser beam at the semiconductor device (Col. 6, line 67 – Col. 7, line 15). For each fuse area 12, a silicon nitride film 6 and silicon oxide film 7 cover the edges of copper regions 2.

2. The Claims Distinguish over Ishimaru

By contrast, claim 7 as amended recites, *inter alia*, insulating portions covering the facing edges of the metal regions of determined pairs according to the specific needs and not covering the facing edges of the metal regions of at least one pair other than the determined pairs .... [and] metal portions connecting the metal regions of the at least one pair other than the determined pairs and not connecting the metal regions of the determined pairs. Ishimaru does not teach or suggest insulating portions that cover the facing edges of some pairs of metal regions but not others. To the contrary, FIG 1 of Ishimaru illustrates that every fuse area 12 of Ishimaru includes a silicon nitride film 6 that covers the facing edges of the copper regions 2. Even if the Office Action considers that the blowing of a fuse may remove the silicon nitride film 6 so as to meet the "not covering" limitation of claim 7, such an interpretation would mean that intact, non-blown fuses would correspond to "determined pairs." However, the claim limitations would still

not be met because claim 7 clearly recites "metal portions not connecting the metal regions of the determined pairs," and Ishimaru clearly shows in FIG. 1 that metal films 8 and 9 do connect the metal regions of intact fuses. For these reasons, claim 7 patentably distinguishes over Ishimaru. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claim 8 depends from claim 7 and is therefore patentable for at least the same reasons.

Claim 9 recites, *inter alia*, insulating portions covering the facing edges of the metal regions of determined pairs and not covering the facing edges of the metal regions of at least one pair other than the determined pairs; and metal portions of the uppermost metallization level which cover the facing edges of the metal regions of all pairs, the metal portions connecting the metal regions of the at least one pair other than the determined pairs and not connecting the metal regions of the determined pairs. As should be appreciated from the above discussion with respect to claim 7, Ishimaru does not teach or suggest these limitations. Therefore, claim 9 patentably distinguishes over Ishimaru. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claim 10 depends from claim 9 and is therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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